UG96&UG95&M95 R2.0

Compatible Design

UMTS/HSPA/GSM/GPRS Module Series

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About the Document

History

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1.0	2015-02-29	Tony GAO	Initial
1.1	2018-09-12	Brooke WANG	1. Added the PCM interface of M95 R2.0. 2. Updated the description of reflow soldering in Chapter 6.1.

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1 Introduction

Quectel UMTS/HSPA UG96&UG95 modules are compatible with Quectel GSM/GPRS M95 R2.0 module. This document briefly describes the compatible design among UG96, UG95 and M95 R2.0 modules.

2 General Descriptions

2.1. Product Description

M95 R2.0 is a quad-band GSM/GPRS module supporting GSM850/EGSM900/DCS1800/PCS1900. UG96 is an UMTS/HSPA module. UG95 is also an UMTS/HSPA module that includes two variants, UG95-A and UG95-E. UG96, UG95 and M95 R2.0 are designed as compatible products, and customers can choose a suitable product according to application requirements. The compatible design guideline ensures a smooth migration from M95 R2.0 to UG96/UG95 modules.

Table 1: Module General Information

Module	Appearance	Packaging	Dimensions (mm)	Description
UG96		102-pin LGA	26.5 × 22.5 × 2.2	UMTS/HSPA module
UG95		102-pin LGA	23.6 × 19.9 × 2.2	UMTS/HSPA module (UG95-A and UG95-E)
M95 R2.0		42-pin LCC	23.6 × 19.9 × 2.65	GSM/GPRS module

2.2. Feature Overview

The following table compares general properties and features of UG96,UG95 and M95 R2.0.

Table 2: Feature Overview

Feature	UG96	UG95	M95 R2.0
Power Supply	3.3V~4.3V Typ. 3.8V	3.3V~4.3V Typ. 3.8V	3.3V~4.6V Typ. 4.0V
Peak Current	VBAT_BB: max 0.8A VBAT_RF: max 2A	VBAT_BB: max 0.8A VBAT_RF: max 2A	VBAT: max 2A
Sleep Current	1.1mA @DRX=5 2.52mA @DRX=6	1.12mA @DRX=5 1.98mA @DRX=6	1.3mA @DRX=5
Frequency Bands	GSM quad-band: 850/900/1800/1900MHz UMTS penta-band: 800/850/900/1900/ 2100MHz	**UG95-A:** Dual band UMTS850/1900MHz **UG95-E:** Dual band GSM900/1800MHz Dual band UMTS900/2100MHz	Quad-band: GSM850/900/1800/ 1900MHz
UMTS/HSPA	Support UMTS/HSPA	Support UMTS/HSPA	Not supported
EDGE	Support EDGE	Downlink only	Not supported
GPRS	Multislot class12	Multislot class12	Multislot class12
GPRS Data Transfer Typical Current (1DL/4UL PCL=5)	GSM850: 601mA EGSM900: 610mA DCS1800: 397mA PCS1900: 434mA	EGSM900: 490mA DCS1800: 335mA	GSM850: 457mA EGSM900: 484mA DCS1800: 461mA PCS1900: 439mA
WCDMA Data Transfer Current (Max Power)	UMTS850/800: 478mA UMTS900: 421mA UMTS1900: 542mA UMTS2100: 480mA	UMTS850: 520mA UMTS900: 512mA UMTS1900: 563mA UMTS2100: 536mA	/
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature

	range: -40°C ~ +90°C	range: -40°C ~ +90°C	range: -40°C ~ +90°C
(U)SIM Interface	1.8V/3.0V (U)SIM	1.8V/3.0V (U)SIM	1.8V/3.0V (U)SIM
UART Interface	**Baudrate:** 300bps~921600bps **Autobauding:** 4800bps~115200bps Flow control: RTS/CTS **Signal level:** 1.8V	**Baudrate:** 300bps~921600bps **Autobauding:** 4800bps~115200bps Flow control: RTS/CTS **Signal level:** 1.8V	**Baudrate:** 300bps~115200bps **Autobauding:** 4800bps~115200bps Flow control: RTS/CTS **Signal level:** 2.8V
USB Interface	USB 2.0 high speed device interface	USB 2.0 high speed device interface	Not supported
Analog Audio	Not supported	Not supported	Two analogy input channels and two analogy output channels
Digital Audio	One Pulse Code Modulation (PCM) digital interface	One Pulse Code Modulation (PCM) digital interface	One Pulse Code Modulation (PCM) digital interface
RTC Backup	Vnorm=1.8V V_I=1.0V~1.9V	Vnorm=1.8V V_I=1.0V~1.9V	$V_O$max=3.0V V_I=1.5V~3.3V
I2C Interface	Supported	Supported	Not supported

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

2.3. Pin Assignment

The following figure shows the pin assignment of UG96, UG95 and M95 R2.0.

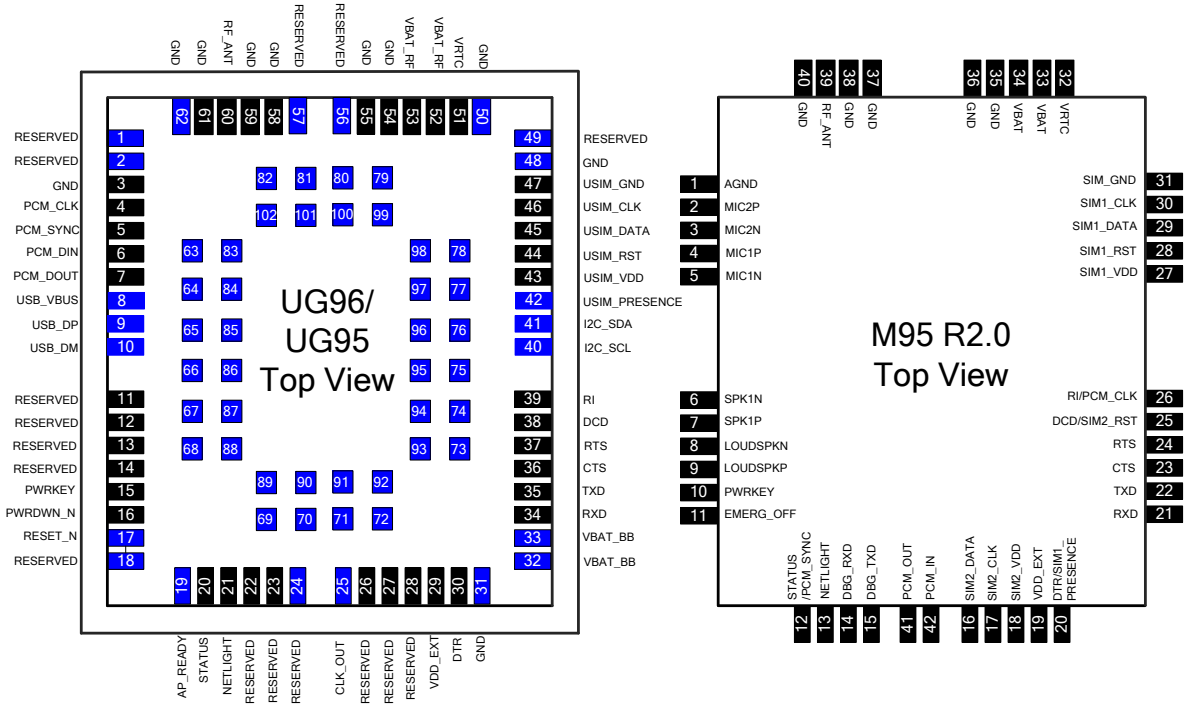


Figure 1: UG96&UG95&M95 R2.0 Pin Assignment

NOTE

The blue pins of UG96&UG95 are the additional pins compared with M95 R2.0.

The following figure shows the combination of pin assignment for UG96, UG95 and M95 R2.0.

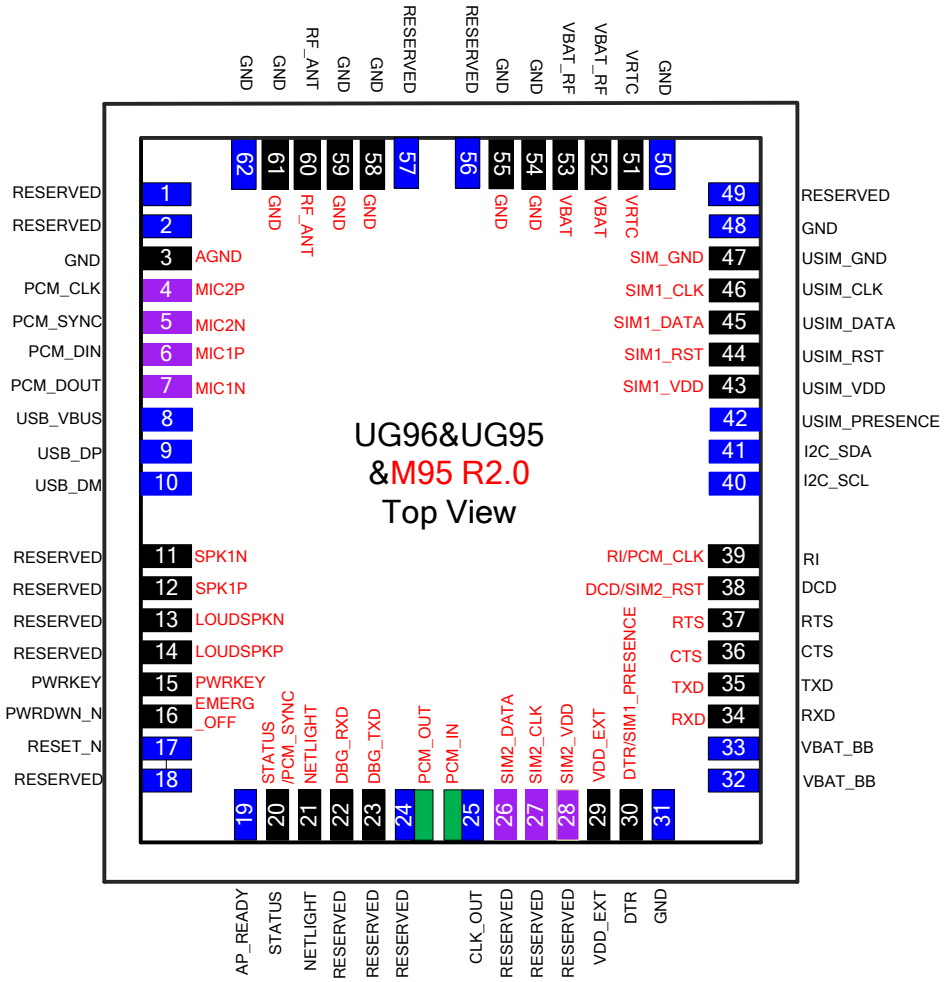


Figure 2: Combined Pin Assignment of UG96&UG95&M95 R2.0

NOTES

1. The blue pins of UG96&UG95 are the additional pins compared with M95 R2.0.
2. The pin names marked in red in the inside area are M95 R2.0's.
3. The black pins of UG96, UG95 and M95 R2.0 are compatible pins in main functions.
4. Due to the different functions of pin 24/25 of UG96&UG95 and the green pins of M95 R2.0, different resistors need to be mounted when using UG96, UG95 or M95 R2.0 for compatible design. For details, please refer to ***document [4]***.
5. The purple pins are different pins in the main functions.

3 Pin Description

This chapter describes the pin definition of UG96, UG95 and M95 R2.0, as well as the pin comparison among them.

Table 3: I/O Parameters Definition

Symbol	Description
IO	Bidirectional
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input
AO	Analog Output
OD	Open Drain

Table 4: Pin Comparison among UG96, UG95 and M95 R2.0

UG96/UG95				M95 R2.0			
Pin No.	Pin Name	IO	Description	Pin No.	Pin Name	IO	Description
1	RESERVED	/	/	/	/	/	/
2	RESERVED	/	/	/	/	/	/
3	GND	/	Ground	1	AGND	/	Ground
4	PCM_CLK	DO	PCM data bit clock. 1.8V power domain.	2	MIC2P	AI	Channel 2 Microphone positive input.

5	PCM_SYNC	DO	PCM data frame sync signal. 1.8V power domain.	3	MIC2N	AI	Channel 2 Microphone negative input.
6	PCM_DIN	DI	PCM data input. 1.8V power domain.	4	MIC1P	AI	Channel 1 Microphone negative input.
7	PCM_DOUT	DO	PCM data output. 1.8V power domain.	5	MIC1N	AI	Channel 1 Microphone negative input.
8	USB_VBUS	PI	USB insertion detection. 2.5V~5.25V.	/	/	/	/
9	USB_DP	IO	USB differential data bus (+)	/	/	/	/
10	USB_DM	IO	USB differential data bus (-)	/	/	/	/
11	RESERVED	/	/	6	SPK1N	AO	Channel 1 Audio negative output.
12	RESERVED	/	/	7	SPK1P	AO	Channel 1 Audio positive output.
13	RESERVED	/	/	8	LOUDSPKN	AO	Channel 2 Audio negative output
14	RESERVED	/	/	9	LOUDSPKP	AO	Channel 2 Audio positive output.
15	PWRKEY	DI	Turn on the module. Pull-up to VRTC by 200KΩ internally.	10	PWRKEY	DI	Turn on/off the module. Pulled up to VBAT.
16	PWRDWN_N	DI	Turn off the module. Use it only when shutdown via AT command cannot be implemented. Pull-up to	11	EMEROG _OFF	DI	Emergency off. Pulled down for at least 40ms, which will turn off the module in case of emergency. Use it only when shutdown via PWRKEY or AT

			VRTC by 4.7KΩ internally.				command cannot be implemented.
17	RESET_N	DI	Reset the module. Pull-up to VRTC by 200KΩ internally.	/	/	/	/
18	RESERVED	/	/	/	/	/	/
19	AP_READY*	DI	Application processor wakeup state input. 1.8V power domain.	/	/	/	/
20	STATUS	DO	Indicate the module's operation status. 1.8V power domain.	12	STATUS/ PCM_SYNC	DO	Indicate the module's operation status. The default function is STATUS after startup. 2.8V power domain.
21	NETLIGHT	DO	Indicate the module's network status. 1.8V power domain.	13	NETLIGHT	DO	Indicate the module's network status. 2.8V power domain.
22	RESERVED	/	/	14	DBG_RXD	DI	Receive data. 2.8V power domain.
23	RESERVED	/	/	15	DBG_TXD	DO	Transmit data. 2.8V power domain.Tra.
24	RESERVED	/	/	41	PCM_OUT	DO	PCM serial data output. 2.8V power domain.
25	CLK_OUT	DO	Provide a digital clock output for an external audio codec.	42	PCM_IN	DI	PCM serial data input. 2.8V power domain.

26	RESERVED	/	/	16	SIM2_DATA	IO	(U)SIM2 card data signal. 1.8V/3.0V
27	RESERVED	/	/	17	SIM2_CLK	DO	(U)SIM2 card clock signal. 1.8V/3.0V 1.8V/3.0V
28	RESERVED	/	/	18	SIM2_VDD	PO	Power supply for (U)SIM2 card. 1.8V/3.0V.
29	VDD_EXT	PO	1.8V	19	VDD_EXT	PO	2.8V
30	DTR	DI	Data terminal ready. Sleep mode control. 1.8V power domain.	20	DTR/ SIM1_ PRESEMCE[1)]	DI	Data terminal ready/ (U)SIM1 card insertion detection. These functions can be switched through AT command.
31	GND	/	Ground	/	/	/	/
32	VBAT_BB	PI	Power supply for module baseband part. 3.3V~4.3V	/	/	/	/
33	VBAT_BB	PI	Power supply for module baseband part. 3.3V~4.3V	/	/	/	/
34	RXD	DI	Receive data. 1.8V power domain.	21	RXD	DI	Receive data. 2.8V power domain.
35	TXD	DO	Transmit data. 1.8V power domain.	22	TXD	DO	Transmit data. 2.8V power domain.
36	CTS	DO	Clear to send. 1.8V power domain.	23	CTS	DO	Clear to send. 2.8V power domain.
37	RTS	DI	Request to send. 1.8V power domain.	24	RTS	DI	Request to send. 2.8V power domain.

38	DCD	DO	Data carrier detection. 1.8V power domain.	25	DCD/ SIM2_RST[2)]	DO	Data carrier detection. (U)SIM2 card reset signal. 2.8V power domain.
39	RI	DO	Ring indicator. 1.8V power domain.	26	RI/ PCM_CLK	DO	Ring indicator/ PCM clock signal. The default function is RI after startup. 2.8V power domain.
40	I2C_SCL	OD	I2C serial clock. 1.8V power domain.	/	/	/	/
41	I2C_SDA	OD	I2C serial data. 1.8V domain.	/	/	/	/
42	USIM_ PRESENCE	DI	(U)SIM card input detection. 1.8V power domain.	/	/	/	/
43	USIM_VDD	PO	Power supply for (U)SIM card. 1.8V/3.0V	27	SIM1_VDD	PO	Power supply for (U)SIM1 card. 1.8V/3.0V
44	USIM_RST	DO	(U)SIM card reset signal. 1.8V/3.0V	28	SIM1_RST	DO	(U)SIM1 card reset signal. 1.8V/3.0V 1.8/3.0V
45	USIM_DATA	IO	(U)SIM card data signal. 1.8V/3.0V	29	SIM1_DATA	IO	(U)SIM1 card data signal. 1.8V/3.0V
46	USIM_CLK	DO	(U)SIM card clock signal. 1.8V/3.0V	30	SIM1_CLK	DO	(U)SIM1 card clock signal. 1.8V/3.0V
47	USIM_GND	/	Ground	31	SIM1_GND	/	Ground
48	GND	/	Ground	/	/	/	/
49	RESERVED	/	/	/	/	/	/
50	GND	/	Ground	/	/	/	/
51	VRTC	PI/ PO	V_O=1.8V. V_I=1.0V~1.9V.	32	VRTC	PI/ PO	$V_O$max=3.0V. $V_O$min=2.0V.

			I_{IN} max=2uA when VBAT is not applied.				$V_O$norm=2.8V. V_I=1.5V~3.3V. Iin≈10uA.
52	VBAT_RF	PI	Power supply for module RF part. 3.3V~4.3V	33	VBAT	PI	Main power supply of module. 3.3V~4.6V
53	VBAT_RF	PI	Power supply for module RF part. 3.3V~4.3V	34	VBAT	PI	Main power supply of module. 3.3V~4.6V
54	GND	/	Ground	35	GND	/	Ground
55	GND	/	Ground	36	GND	/	Ground
56	RESERVED	/	/	/	/	/	/
57	RESERVED	/	/	/	/	/	/
58	GND	/	Ground	37	GND	/	Ground
59	GND	/	Ground	38	GND	/	Ground
60	RF_ANT	IO	RF antenna.	39	RF_ANT	IO	RF antenna.
61	GND	/	Ground	40	GND	/	Ground
62	GND	/	Ground	/	/	/	/
63~66, 75~78, 83~88, 92~99	RESERVED	/	/	/	/	/	/
67~74, 79~82, 89~91, 100~102	GND	/	Ground	/	/	/	/

NOTES

1. The blue pins of UG96&UG95 are the additional pins compared with M95 R2.0.
2. The pins marked in red are compatible pins, but their functions are different.
3. The black pins are compatible pins in main functions.
4. Keep all reserved and unused pins unconnected.
5. All GND pins should be connected to ground.

6. The AGND pin of M95 R2.0 should be routed as single-ended to main ground when analog audio is used in single-ended application. Otherwise, it can be connected to GND directly.
7. "*" means under development.
8. 1) DTR pin can be used as SIM1_PRESENCE pin via AT command. For more details, please refer to ***document [3]***.
9. 2) When (U)SIM2 interface is used, DCD pin can be used as SIM2_RST pin. For more details, please refer to ***document [5]***.

4 Hardware Reference Design

The following chapters describe compatible design among UG96, UG95 and M95 R2.0 on main functions.

4.1. Power Supply

4.1.1. Power Supply Reference Design

Power design for a module is critical to its performance. The power supply of UG96, UG95 and M95 R2.0 should be able to provide sufficient current up to 2.0A. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supply is about 3.8V and the maximum load current is 3.0A.

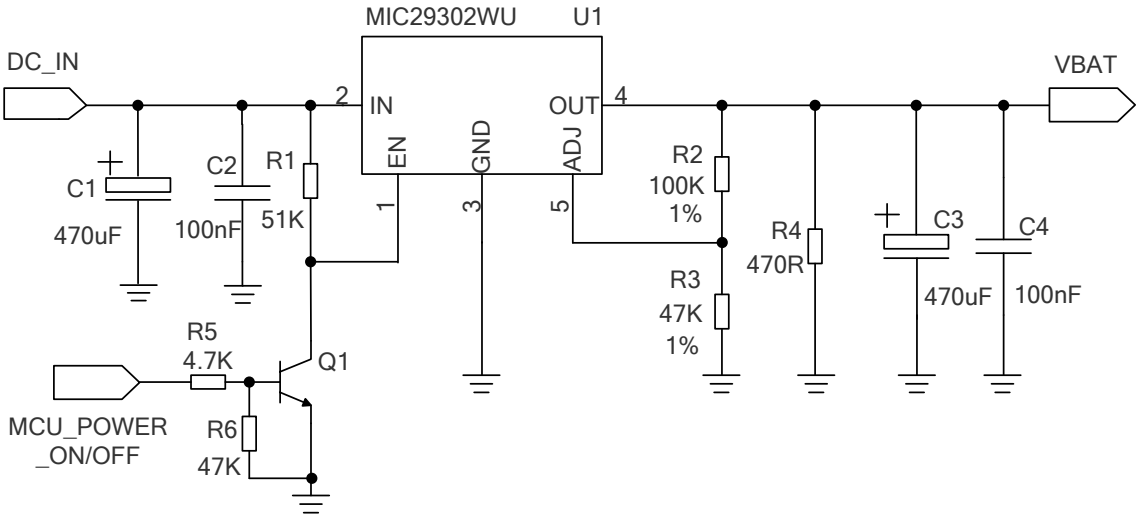


Figure 3: Reference Circuit Design of Power Supply

4.1.2. Decrease Voltage Drop

The power supply range of UG96/UG95 is 3.3V~4.3V and the power supply range of M95 R2.0 is 3.3V~4.6V. Please make sure that the input voltage will never drop below 3.3V and exceed 4.3V, and the typical power supply is 3.8V. The VBAT to UG96/UG95's VBAT_BB and VBAT_RF pins should be divided into two separated paths in star structure.

In addition, in order to get a stable power source, it is recommended to use a zener diode with reverse zener voltage of 5.1V and dissipation power more than 0.5W.

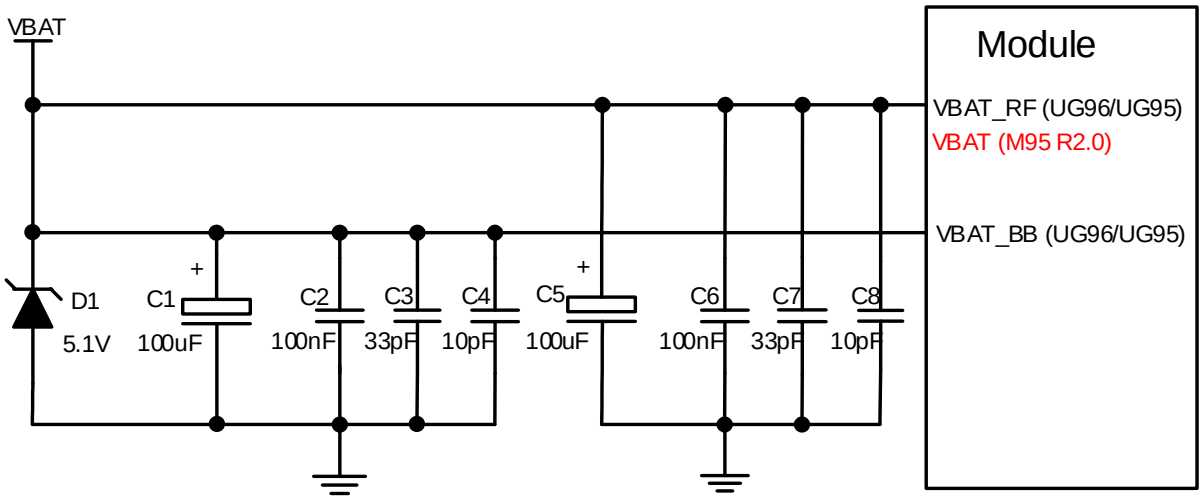


Figure 4: Reference Circuit Design of Star Structure

M95 R2.0 only has two pads for VBAT input, and this is different from UG96/UG95. Therefore, it is not recommended to mount C1~C4. VBAT_RF pins of UG96/UG95 are compatible with VBAT pins of M95 R2.0.

4.2. Power-on Circuit

UG96/UG95 and M95 R2.0 can be turned on by driving the PWRKEY pin to a low level, though the power domain of the pin of M95 R2.0 is different from UG96/UG95.

The following circuit is a reference design for turning on the module using PWRKEY.

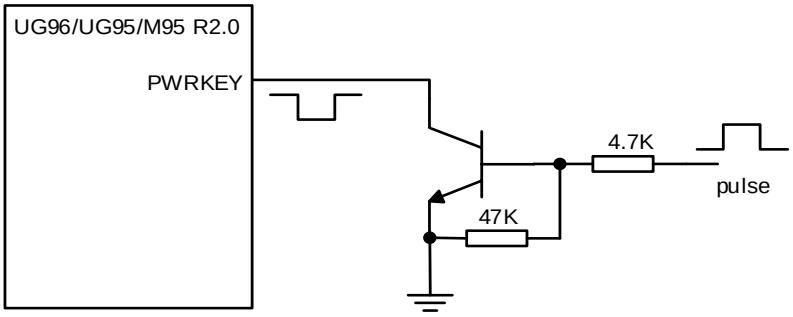


Figure 5: Turn on the Module Using PWRKEY Driving Circuit

The power-on scenario is illustrated as the following figure.

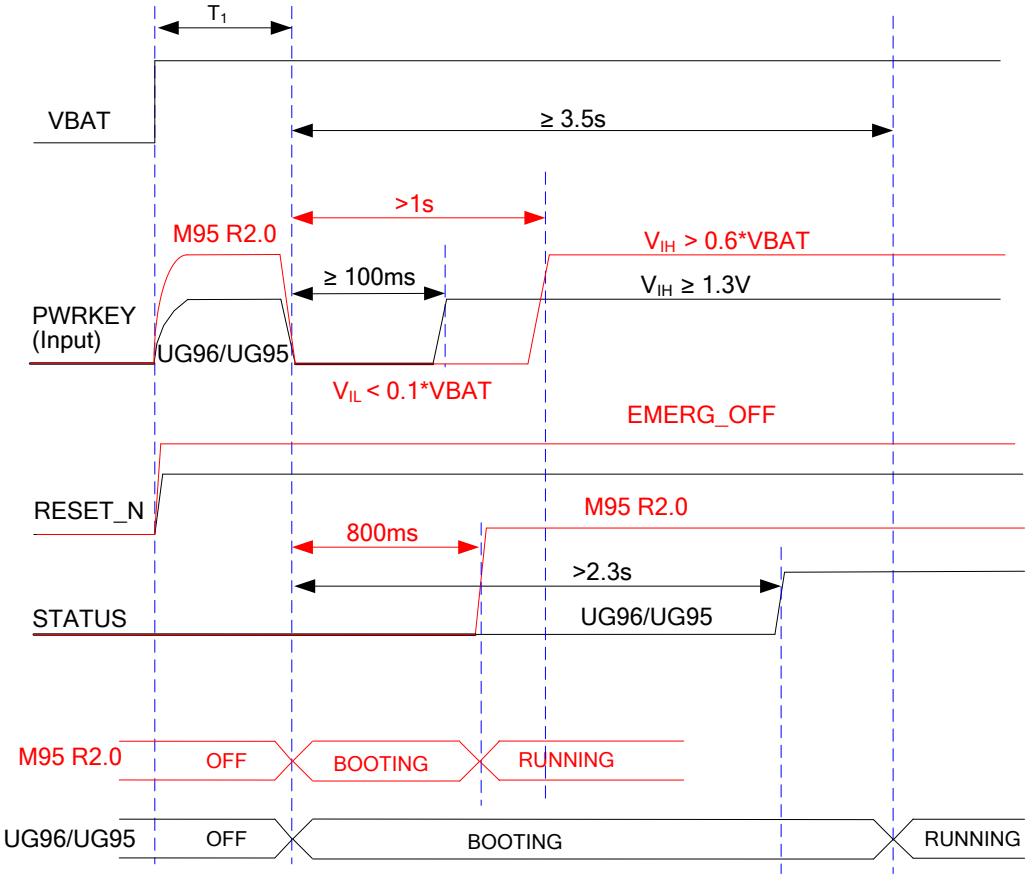


Figure 6: Power-on Scenario

NOTES

1. When UG96/UG95 is turned on through driving PWRKEY to a low level, please make sure that VBAT is stable before pulling down PWRKEY pin. The recommended time of T_1 is 100ms. PWRKEY cannot be pulled down all the time.

2. The time of pulling down PWRKEY of UG96/UG95 and M95 R2.0 is different.
3. The parts marked in black in the above figure are for UG96/UG95.
4. The parts marked in red in the above figure are for M95 R2.0.

4.3. Power-off Circuit

4.3.1. Turn off Module Using AT Command

There are several different ways to turn off UG96/UG95 and M95 R2.0. It is recommended to use a safe way to turn off the module by **AT+QPOWD**, which will let the module log off from the network and allow the firmware to save important data before completely disconnecting the power supply.

The power-off scenario is illustrated as the following figure.

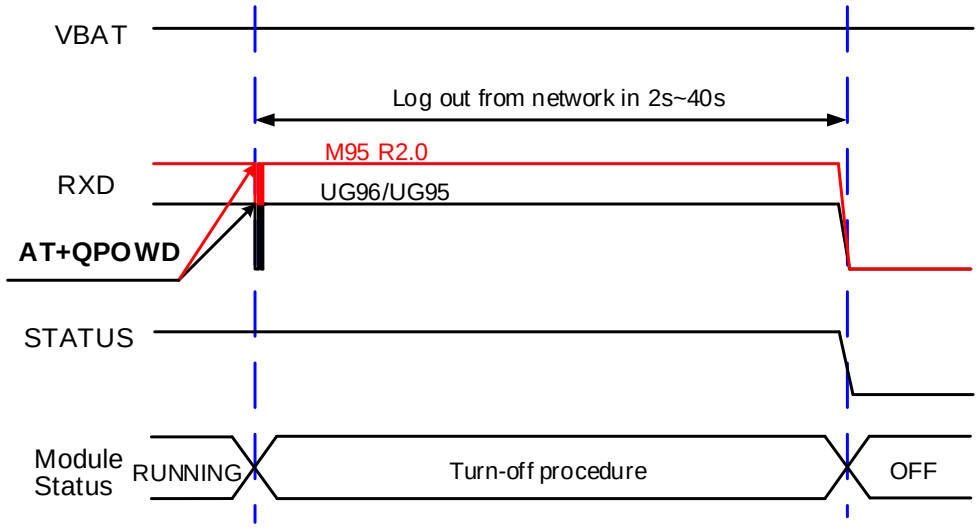


Figure 7: Power-off Scenario

NOTES

1. The parts marked in black in the above figure are for UG96/UG95.
2. The parts marked in red in the above figure are for M95 R2.0.
3. Network logout time is related to local network signal strength.

4.3.2. Turn off M95 R2.0 Using PWRKEY Pin

It is also a safe way to turn off M95 R2.0 by pulling down the PWRKEY pin for a period of time (0.7s~1s), while UG96/UG95 cannot be turned off by the PWRKEY pin.

The power-off scenario is illustrated as the following figure.

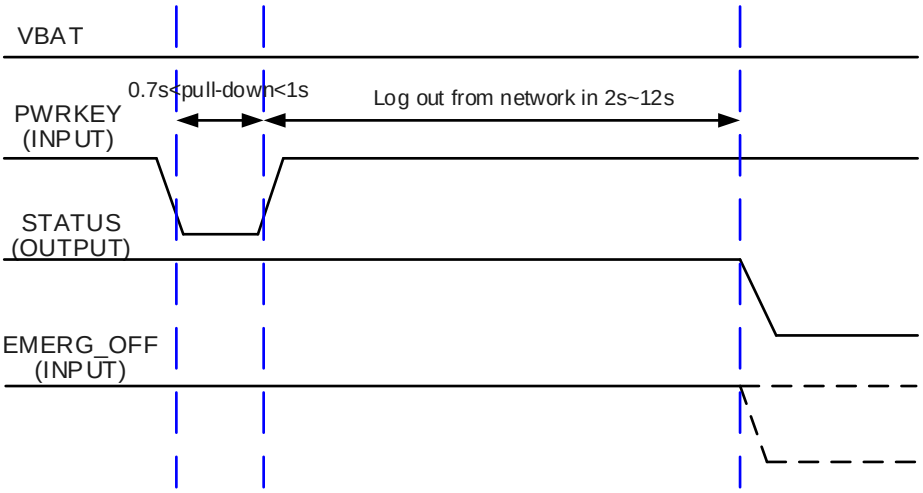


Figure 8: M95 R2.0's Power-off Scenario

NOTE

Network logout time is related to local network signal strength.

4.3.3. Emergency Shutdown

UG96/UG95 can be shut down by PWRDWN_N pin and M95 R2.0 can be shut down by EMERG_OFF pin. The two pins should only be used under emergency situations, such as when the module crashes or works abnormally. Although turning off the module by PWRDWN_N or EMERG_OFF is fully tested and nothing wrong detected, this operation is still a big risk as it could cause destroying of the code or data area of the flash memory in the module. Therefore, it is recommended that PWRKEY or AT command should always be the preferential way to turn off the module.

The following circuit is a reference design for UG96/UG95 and M95 R2.0's emergency shutdown.

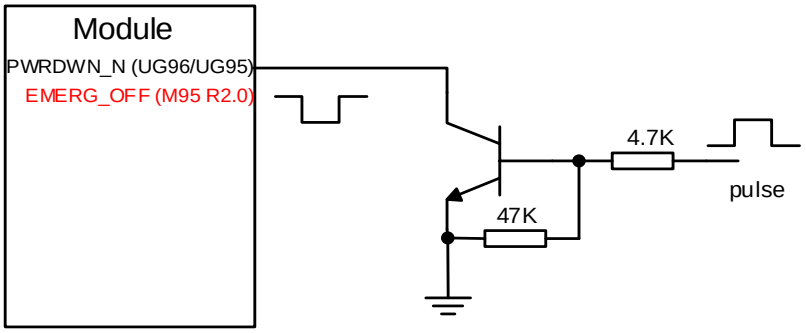


Figure 9: Driving Circuit of Emergency Shutdown

The emergency shutdown scenario is illustrated as the following figure.

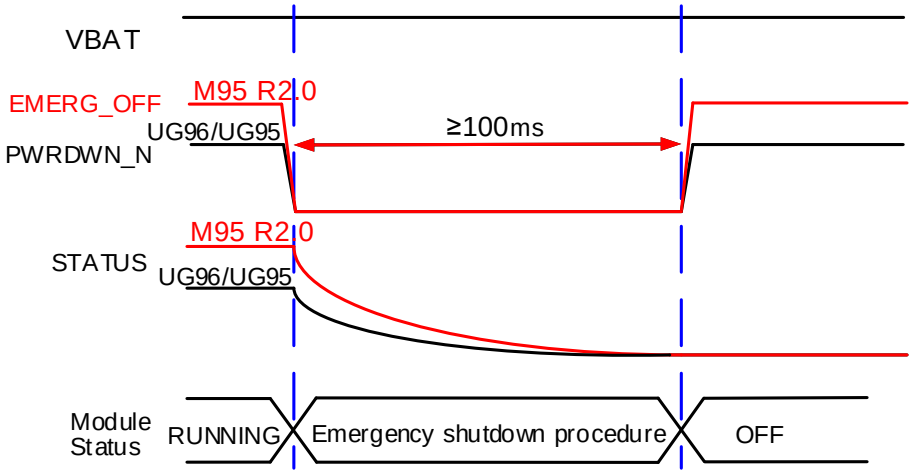


Figure 10: Emergency Shutdown Scenario

4.4. Network Status Indication

The NETLIGHT signal can be used to drive a network status indicator LED, so as to indicate the network status of UG96/UG95/M95 R2.0. A reference design is shown as below.

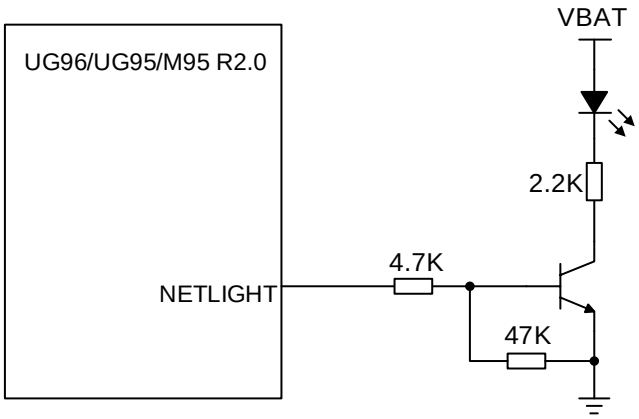


Figure 11: Reference Circuit of NETLIGHT

4.5. Operation Status Indication

The STATUS pin is set as the module's operation status indicator. It will output high level when module is powered on. The following figure shows the reference design of driving LED for STATUS.

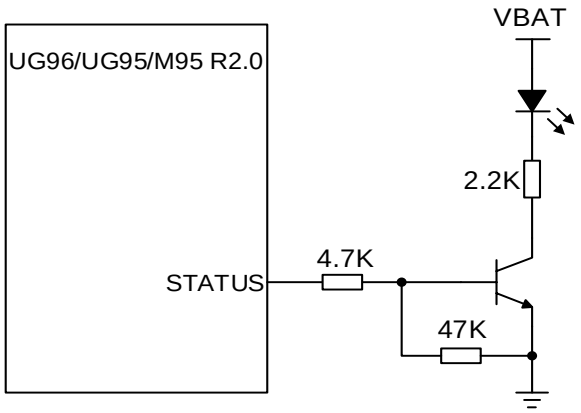


Figure 12: Reference Circuit of STATUS

4.6. (U)SIM Interface

(U)SIM interface of UG96/UG95 and M95 R2.0 supports 1.8V or 3.0V USIM/SIM cards by default. The pin assignment of UG96/UG95's (U)SIM interface is compatible with that of the M95 R2.0's (U)SIM1 interface, except that UG96/UG95's pin SIM1_PRESENCE is not compatible with M95 R2.0's USIM_PRESENCE.

A reference design of 6-pin (U)SIM interface is shown in the figure below:

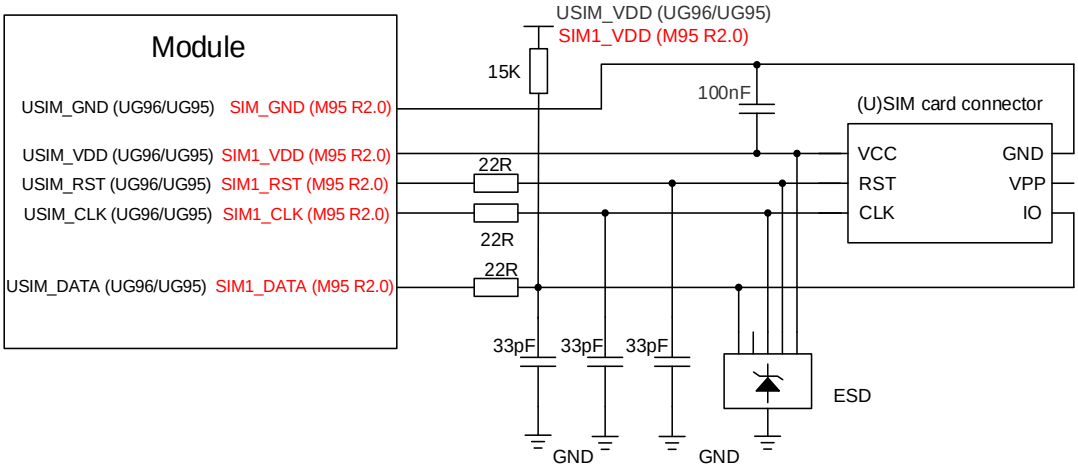


Figure 13: Reference Design of 6-Pin (U)SIM Interface

If (U)SIM card detection function is used, keep SIM1_PRESENCE or USIM_PRESENCE pin connected. A reference design for 8-pin (U)SIM interface is shown in the figure below:

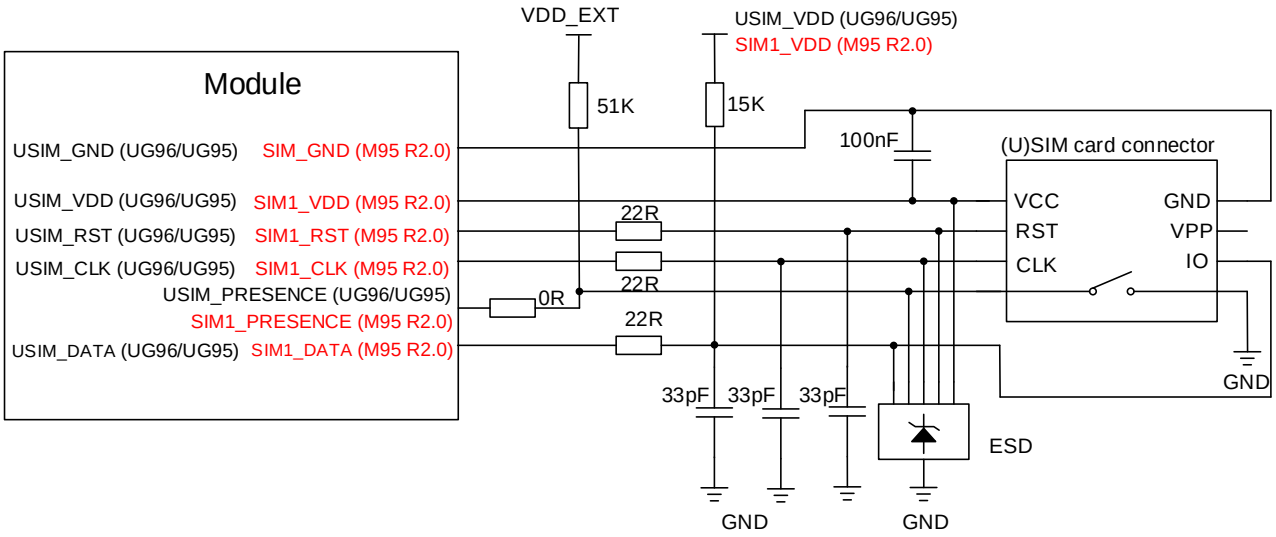


Figure 14: Reference Design of 8-Pin (U)SIM Interface

4.7. UART Interface

UG96, UG95 and M95 R2.0 support UART interface. The following circuit shows the reference design for main UART interface level matching. It is recommended to add a level matching circuit between UG96/UG95/M95 R2.0 module and MCU due to the different power domain of UART interfaces. For details, please refer to ***document [1]*** & ***[2]***.

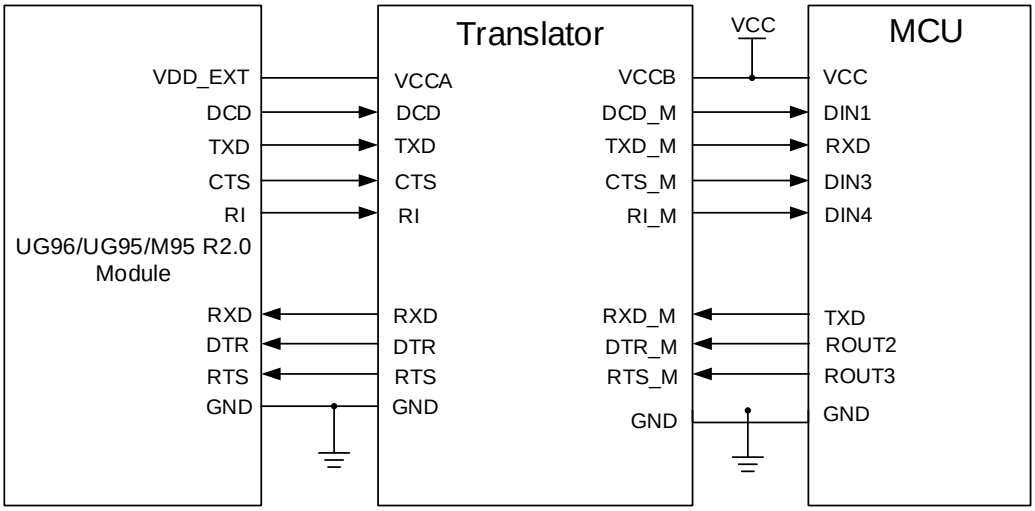


Figure 15: Reference Design of Main UART Interface

NOTES

1. UG96/UG95's UART pins belong to 1.8V power domain.
2. M95 R2.0's UART pins belong to 2.8V power domain.
3. It is recommended to reserve USB_DP, USB_DM and USB_VBUS pins as test points and then place them on DTE for debugging.

4.8. USB Interface

UG96/UG95 provides one integrated Universal Serial Bus (USB) interface, which complies with the USB 2.0 specifications and supports high speed (480Mbps) and full speed (12Mbps) modes on USB 2.0. It supports USB device only.

If application processor communicates with UG96/UG95 via USB interface and communicates with M95 R2.0 via UART interface, the reference design for UG96/UG95's USB interface and M95 R2.0's main UART interface is shown as the following figure.

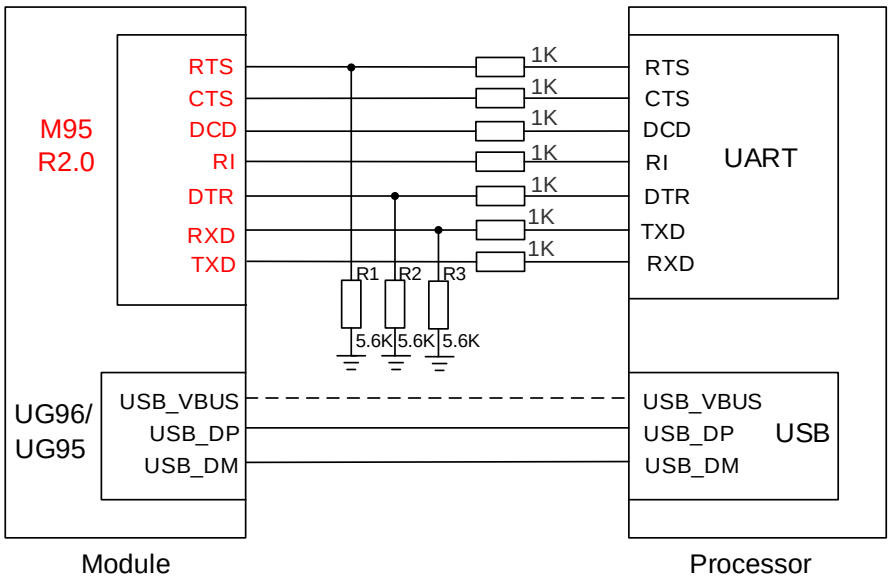


Figure 16: Reference Design of USB Interface (UG96/UG95) and UART Interface (M95 R2.0)

NOTES

1. The resistance 5.6K is used on 3.3V IO level system. While on 3V IO level system, the resistance of R1~R3 should be changed to 10KΩ, and the max input voltage to module should be 2.8V.
2. Please pay attention to the voltage level matching between the module and processor. For details, please refer to ***document [4]***.

4.9. Audio Interfaces

M95 R2.0 provides two analogy input channels, two analogy output channels and one PCM interface, while UG96/UG95 only provides one PCM audio interface.

The following figure shows the compatible reference design of audio interfaces. For more details, please refer to ***document [1]***, ***[2]*** and ***[3]***.

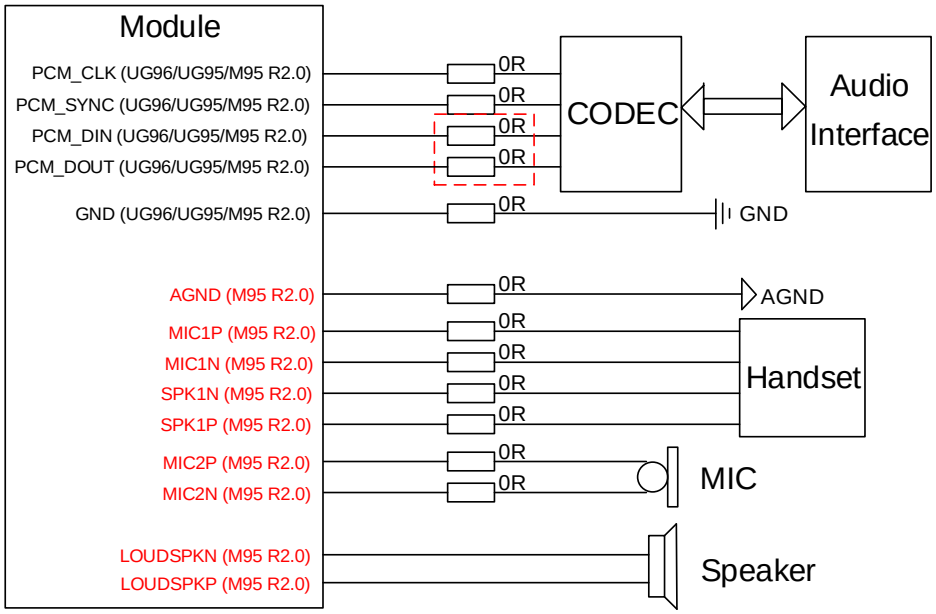


Figure 17: Reference Design of Audio Interfaces

NOTE

For more details of audio interface compatible design, please refer to ***document [4]***.

4.10. RF Interface

RF_ANT is a compatible pin among UG96/UG95 and M95 R2.0. The impedance of the RF interface is 50Ω.

In order to achieve better RF performance, it is recommended to reserve a π-type matching circuit (R1/C1/C2) and place it close to the antenna. The capacitors (C1/C2) are not mounted and a 0Ω resistor is mounted on R1 by default. A reference design for RF antenna interface is shown as below.

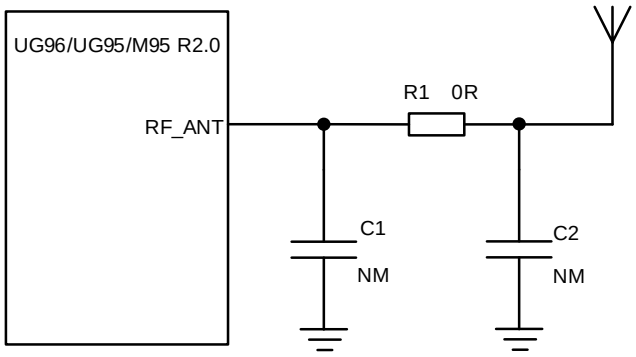


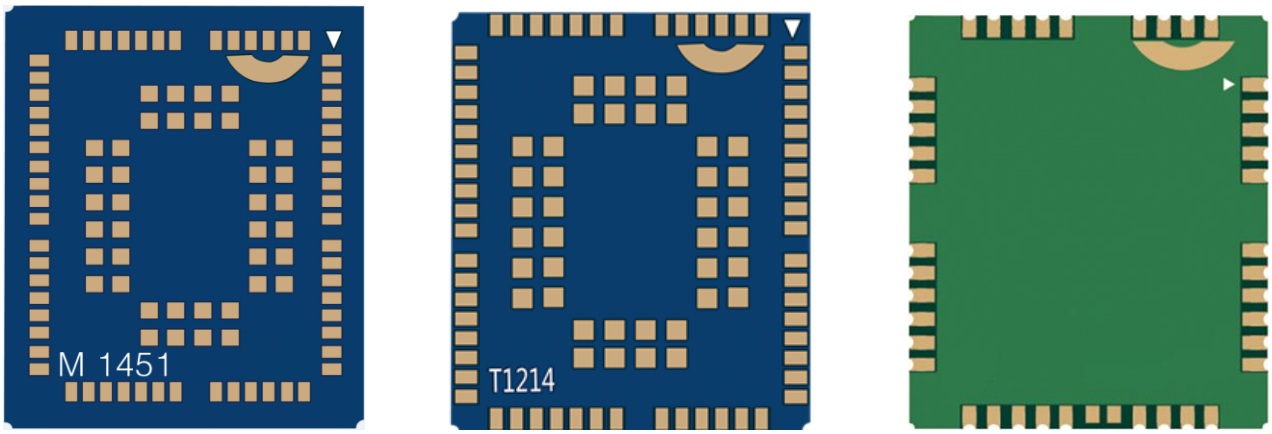
Figure 18: Reference Design of RF Interface

5 Recommended Footprint and Stencil Design

This chapter mainly introduces the recommended compatible footprint and stencil design of UG96, UG95 and M95 R2.0. All dimensions are measured in millimeter (mm), and the tolerances for dimensions without tolerance values are ±0.05mm.

5.1. Recommended Compatible Footprint

The following figure shows the bottom views of UG96, UG95 and M95 R2.0.



UG96 **UG95** **M95 R2.0**

Figure 19: Bottom Views of UG96/UG95/M95 R2.0

The following figure shows the recommended compatible footprint of UG96, UG95 and M95 R2.0.

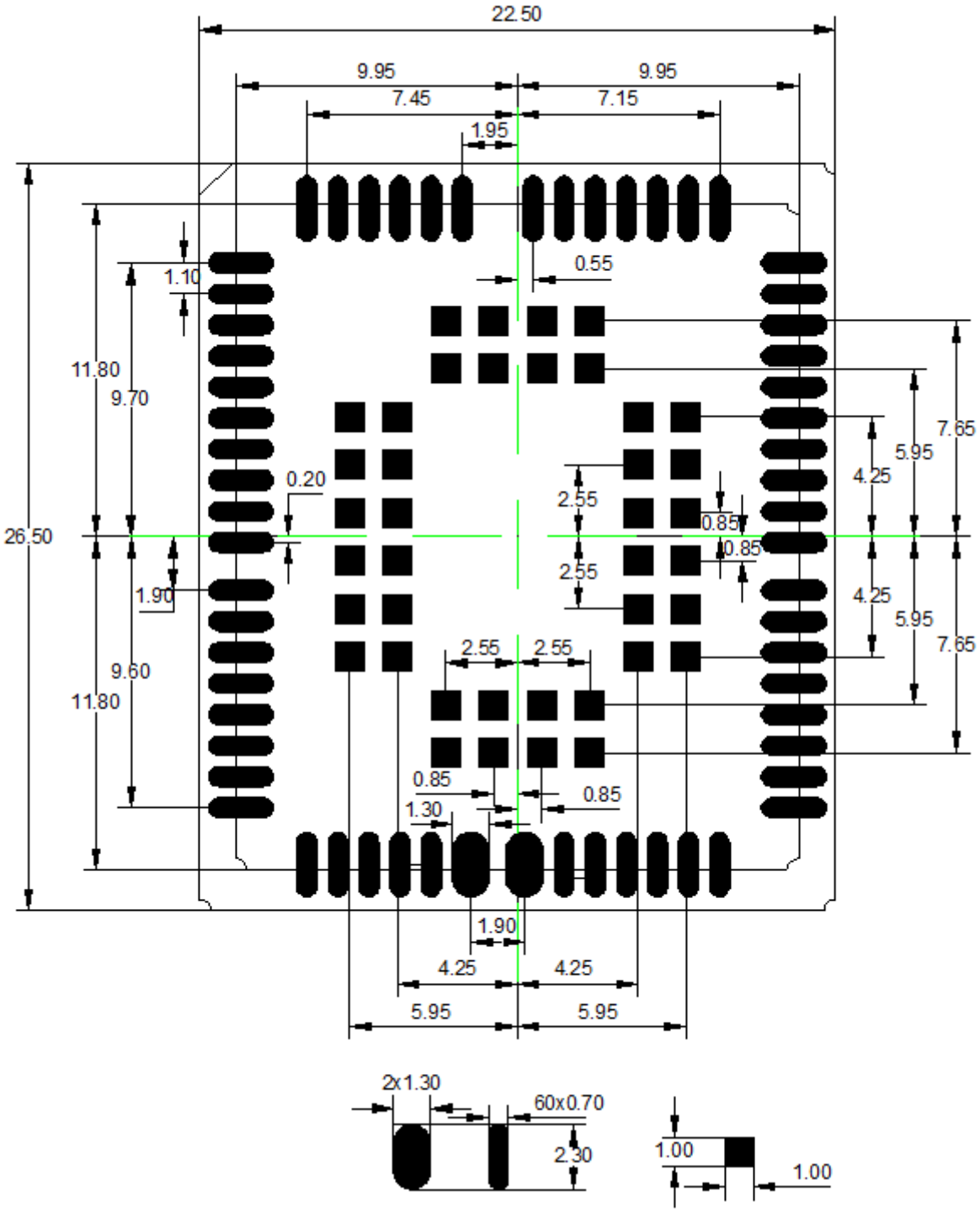


Figure 20: Recommended Footprint of UG96/UG95/M95 R2.0

5.2. Recommended Stencil Design

UG96, UG95 and M95 R2.0 have different PCB thicknesses. In order to ensure the module soldering quality, the thickness of stencil is recommended to be 0.13mm for UG96/UG95 and 0.2mm for M95 R2.0. For more details, please refer to ***document [6]***.

The recommended stencil design of UG96 is shown as below.

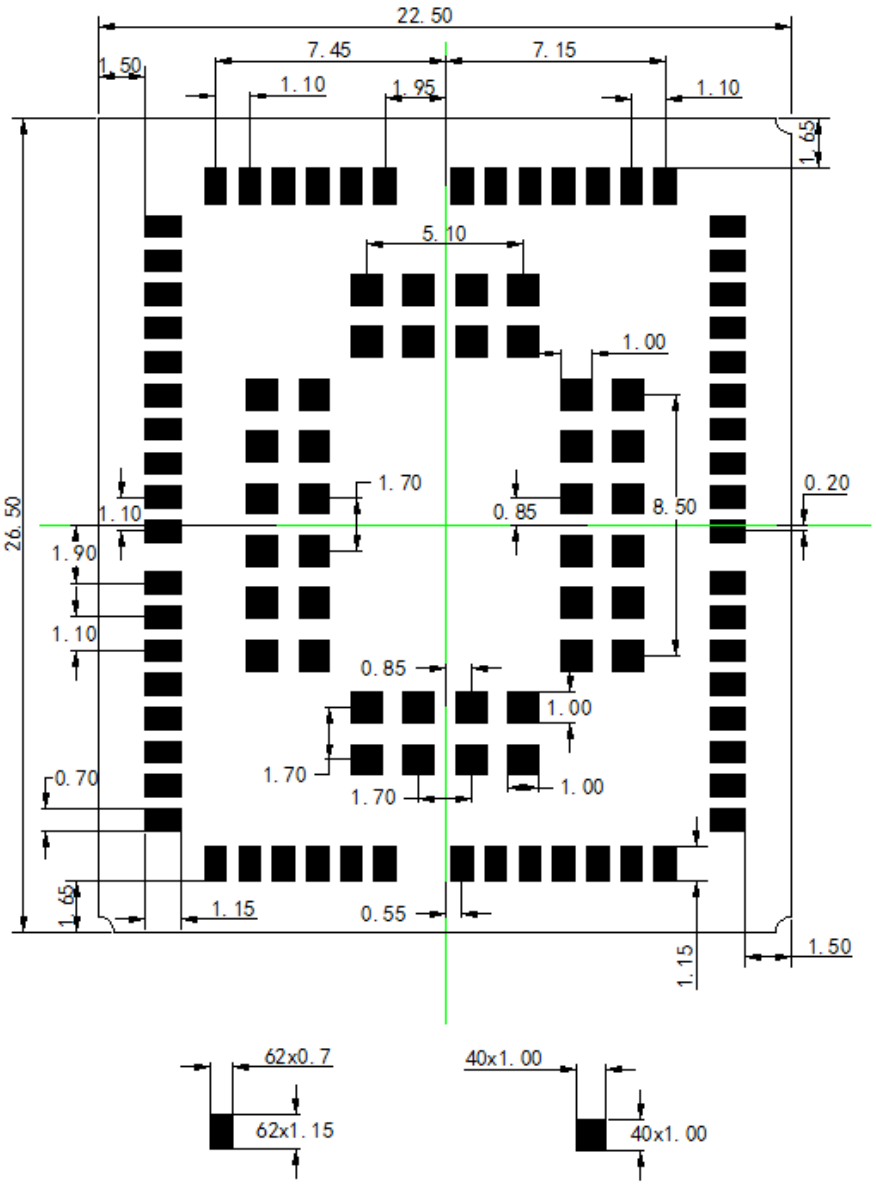


Figure 21: Recommended Stencil Design of UG96

The recommended stencil design of UG95 is shown as below.

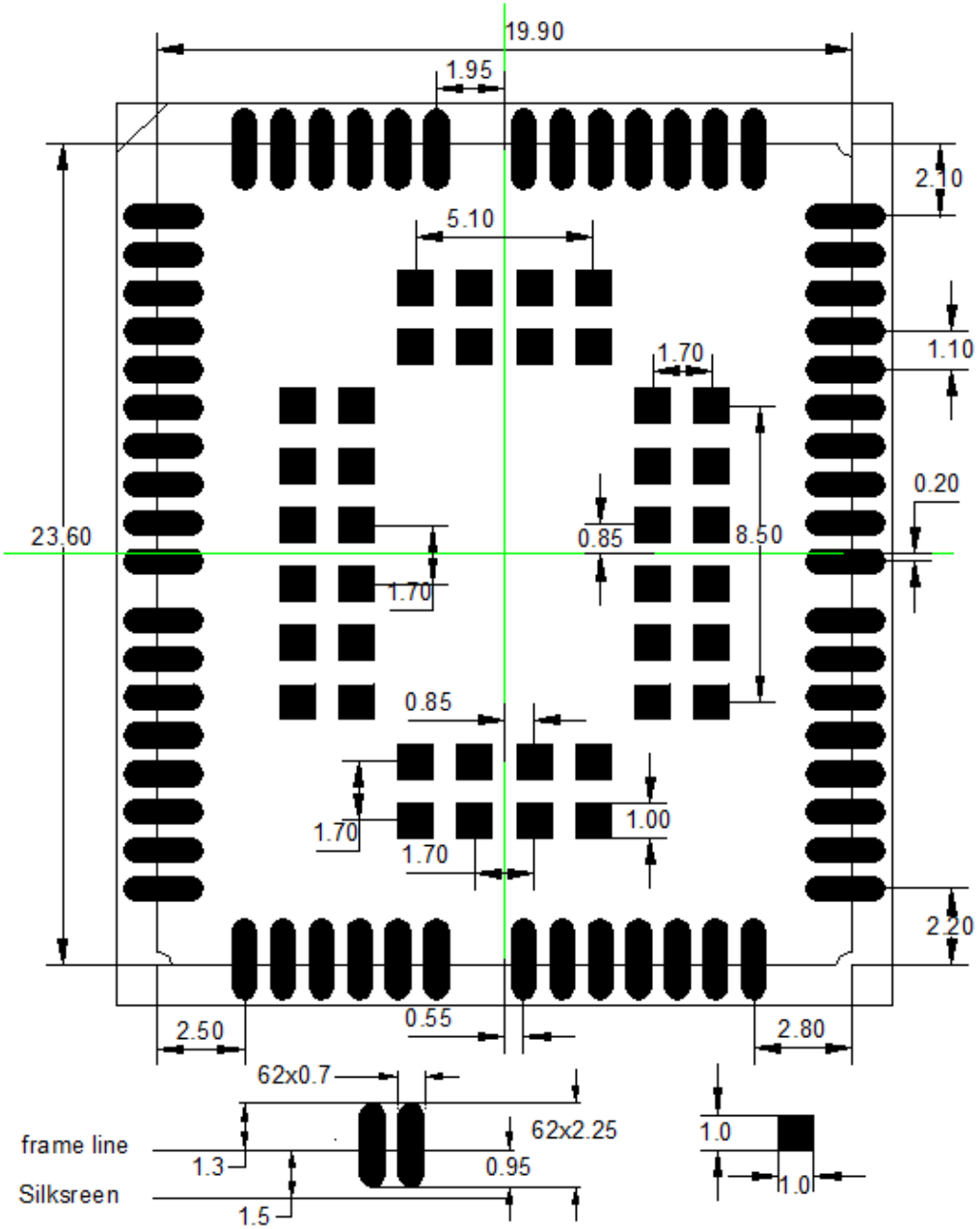


Figure 22: Recommended Stencil Design of UG95

The recommended stencil design of M95 R2.0 is shown as below.

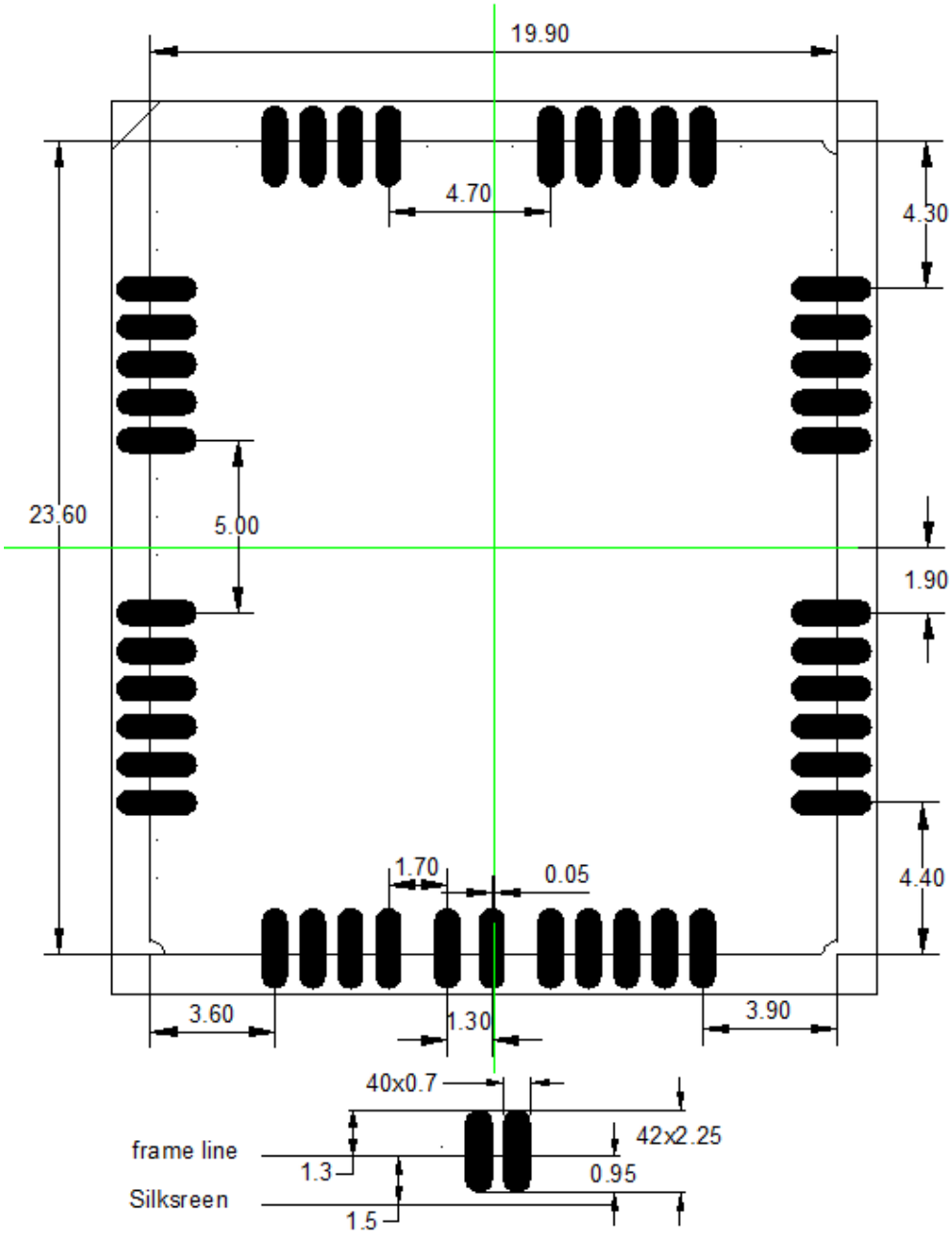


Figure 23: Recommended Stencil Design of M95 R2.0

5.3. Installation Sketch Map

The following figure shows the sketch map of installation for UG96, UG95 and M95 R2.0.

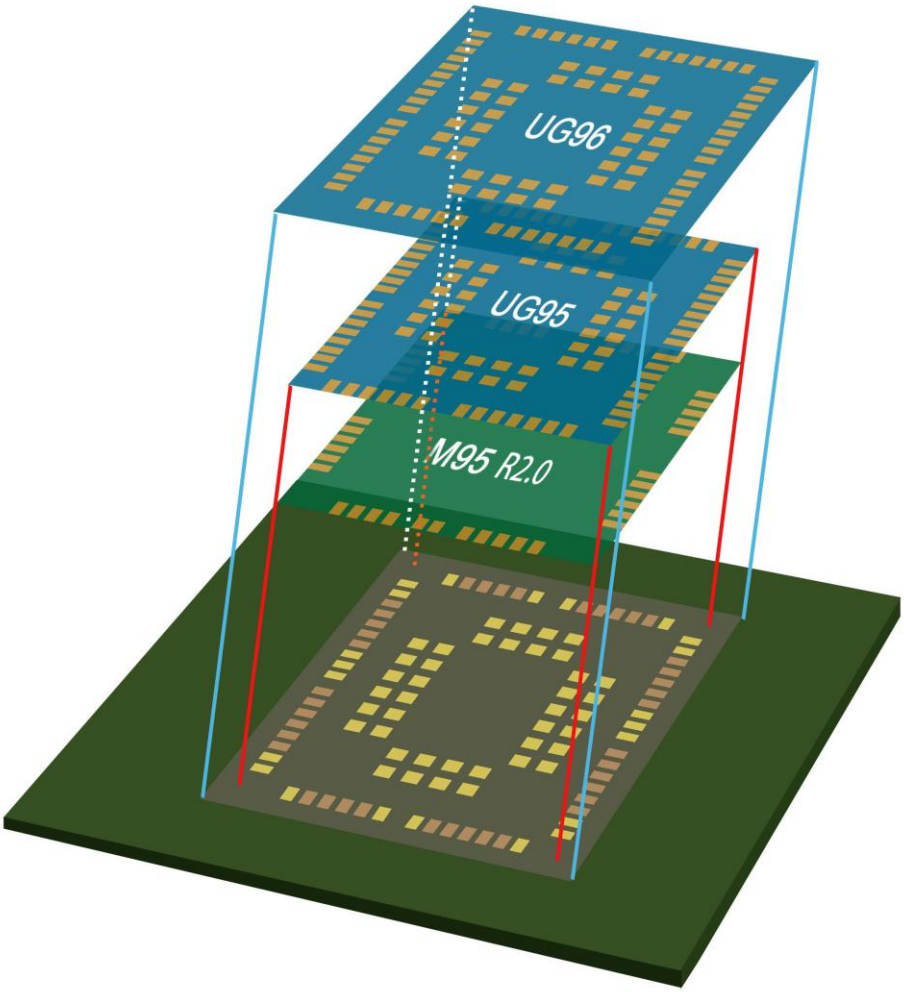


Figure 24: Installation Sketch Map for UG96/UG95/M95 R2.0

6 Manufacturing and Packaging

6.1. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil is recommended to be 0.13mm for UG96/UG95 and 0.2mm for M95 R2.0. For more details, please refer to ***document [6]***.

It is suggested that the peak reflow temperature is 240ºC~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

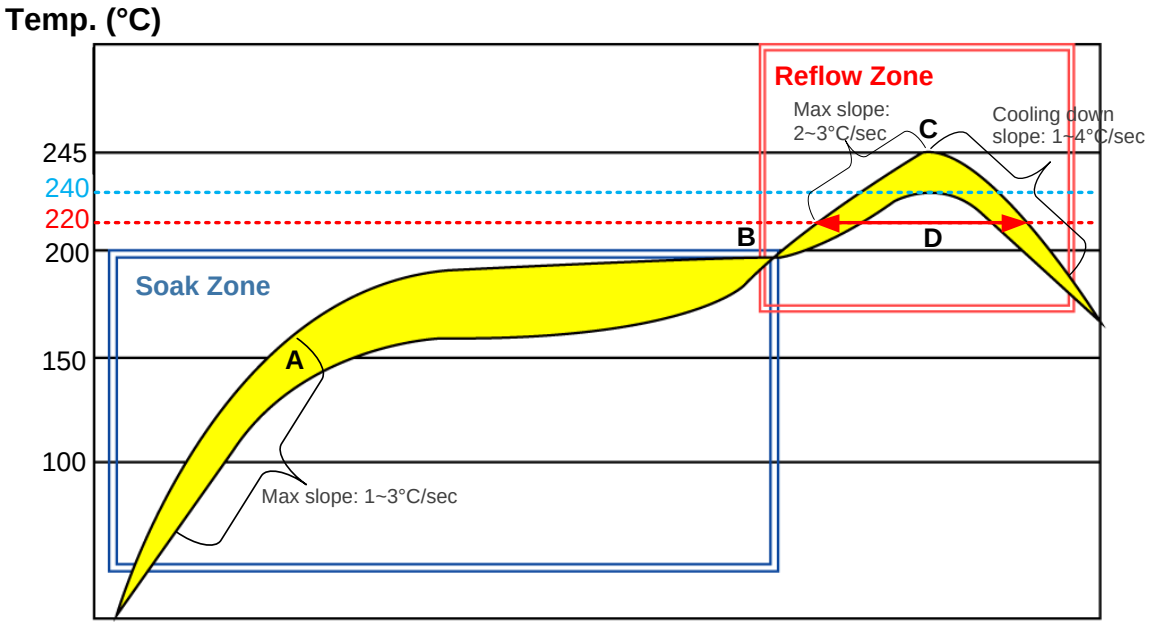


Figure 25: Recommended Reflow Soldering Thermal Profile

Table 5: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec
Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	240°C~245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the 2D barcode is still readable, although white rust may be found.

6.2. Packaging

UG96, UG95 and M95 R2.0 modules adopt tape and reel packaging and are stored in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The reel is 330mm in diameter and each reel contains 250 modules. The following figures show the packaging details, measured in mm.

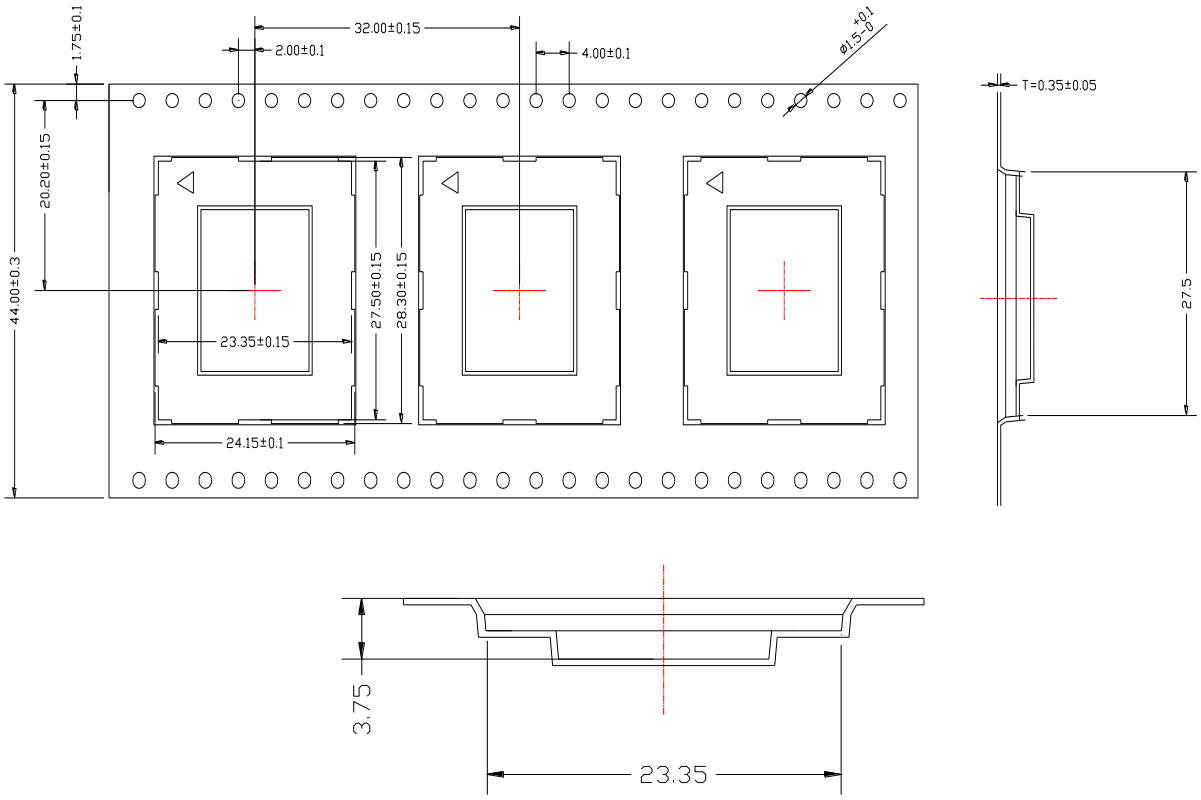


Figure 26: Tape Dimensions of UG96

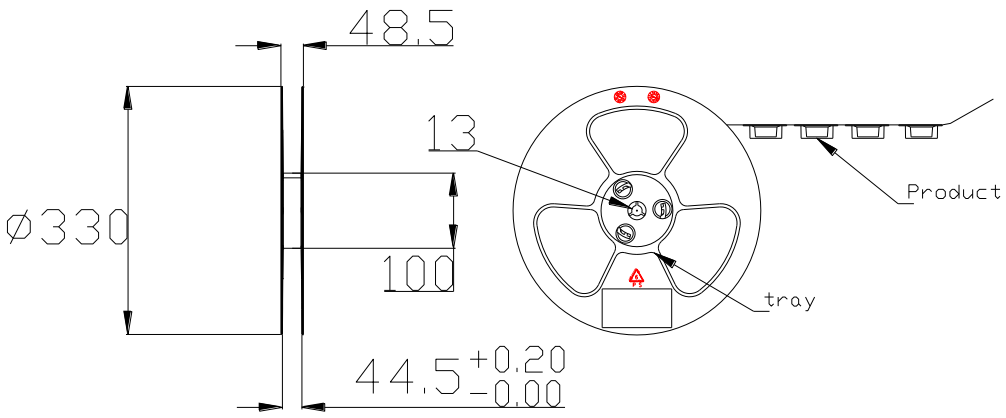


Figure 27: Reel Dimensions of UG96

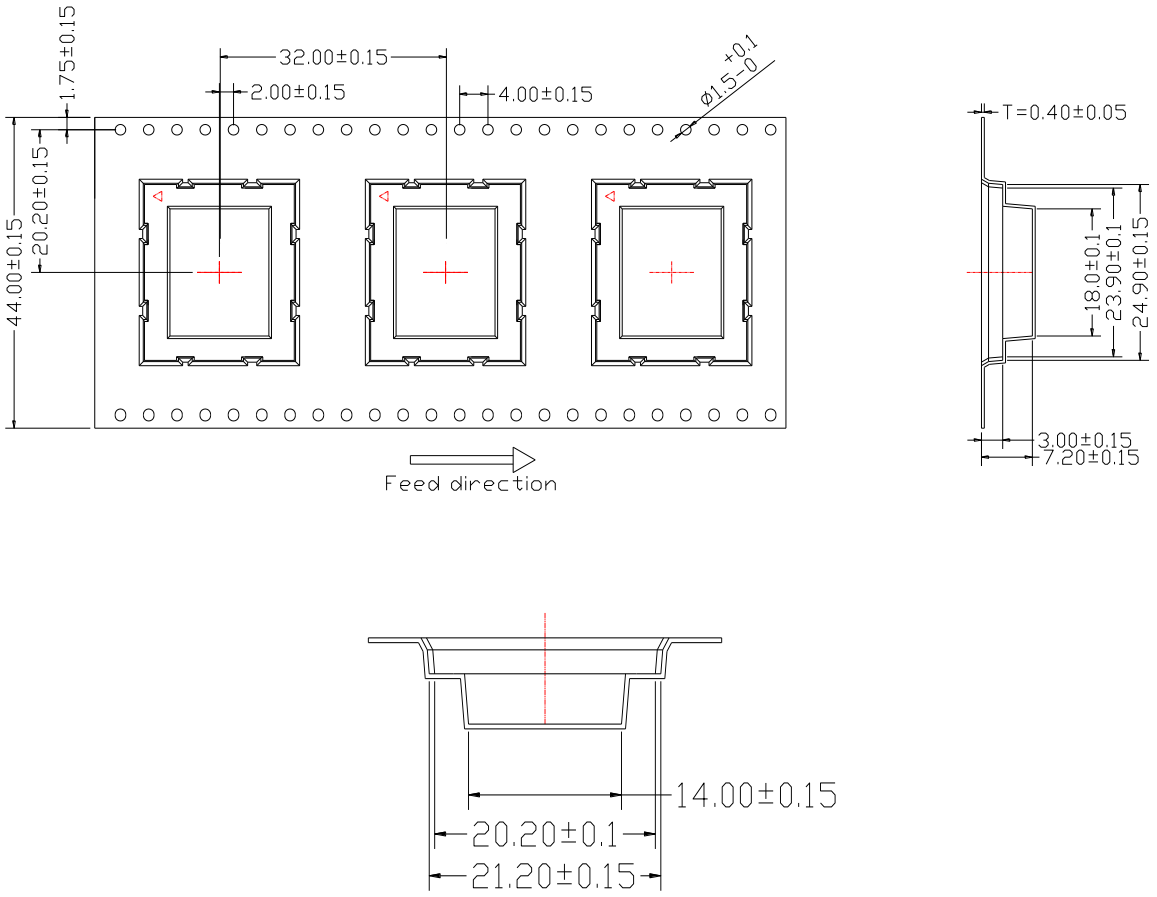


Figure 28: Tape Dimensions of UG95/M95 R2.0

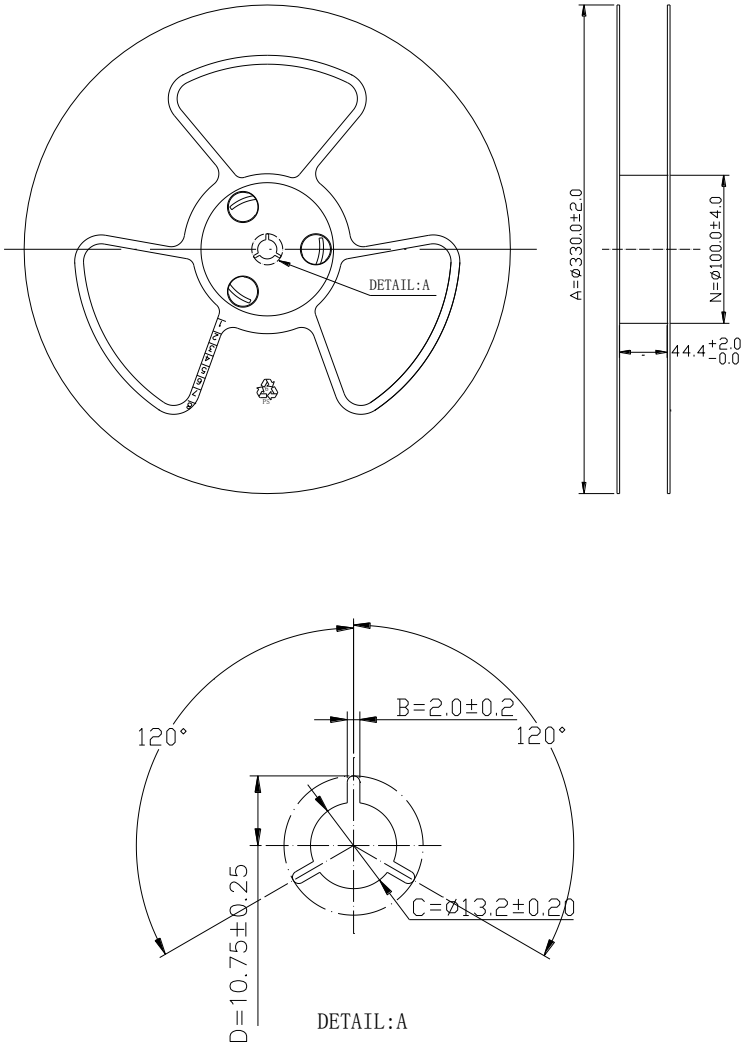


Figure 29: Reel Dimensions of UG95/M95 R2.0

Table 6: Reel Packing

Model Name	MOQ for MP	Minimum Package: 250pcs	Minimum Package×4=1000pcs
UG96	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.78kg G.W: 1.46kg	Size: 380mm × 250mm × 365mm N.W: 3.1kg G.W: 6.45kg
UG95/M95 R2.0	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.63kg G.W: 1.41kg	Size: 380mm × 250mm × 365mm N.W: 2.5kg G.W: 6.25kg

7 Appendix A References

Table 7: Related Documents

SN	Document Name	Remark
[1]	Quectel_UG96_Hardware_Design	UG96 Hardware Design
[2]	Quectel_UG95_Hardware_Design	UG95 Hardware Design
[3]	Quectel_M95_Hardware_Design	M95 Hardware Design
[4]	Quectel_UG96&UG95&M95 R2.0_Reference_Design	UG96, UG95 and M95 R2.0 Reference Design
[5]	Quectel_M95_Dual_SIM_Application_Note	M95 Dual SIM Application Note
[6]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide

Table 8: Terms and Abbreviations

Abbreviation	Description
bps	Bits Per Second
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
ESD	Electrostatic Discharge
HSPA	High Speed Packet Access
LCC	Leadless Chip Carriers
LDO	Low Dropout Regulator
LED	Light Emitting Diode

LGA	Land Grid Array
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCS	Personal Communication System
RF	Radio Frequency
RI	Ring Indicator
RTC	Real Time Clock
RTS	Require To Send
Rx	Receive
RXD	Receive Direction
SMS	Short Message Service
SMT	Surface Mount Technology
TX	Transmitting Direction
TXD	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
(U)SIM	(Universal) Subscriber Identification Module
UMTS	Universal Mobile Telecommunications System
WCDMA	Wideband Code Division Multiple Access